7. (Previously amended) A semiconductor substrate including at least one adhesive patch comprised of a viscous adhesive material, the at least one adhesive patch including a first surface adjacent said semiconductor substrate and a second, smaller surface opposite said first surface exhibiting a generally planar portion over a substantial portion thereof, said semiconductor substrate including said at least one adhesive patch formed by:

providing a semiconductor substrate;

dispensing a viscous adhesive material on said semiconductor substrate; and

inverting said semiconductor substrate without effecting substantial lateral confinement of said adhesive material and maintaining said semiconductor substrate in an inverted position at least until said viscous adhesive material sufficiently stabilizes so as to exhibit a desired stable shape and a lateral boundary defining sizes of said first and second surfaces of said at least one adhesive patch and wherein at least a substantial portion of said second, smaller surface of said adhesive patch exhibits a generally planar configuration and said size of said second, smaller surface is smaller than said size of said first surface.

8. (Previously amended) The semiconductor substrate of claim 7, wherein dispensing said viscous adhesive material, comprises:

placing a template, including at least one aperture, on said semiconductor substrate;

depositing said adhesive material into said at least one aperture; and

removing said template prior to substantially inverting said semiconductor substrate.

15. (Previously twice amended) A flip-chip including at least one conductive bump comprised of a viscous conductive material, the at least one conductive bump exhibiting a height-to-width ratio of at least approximately 3 to 1 and including a first surface adjacent said flip-chip and a second surface opposite said first surface exhibiting a generally planar portion over a substantial portion thereof, said flip chip including said at least one conductive bump formed by:

providing said flip-chip with at least one bond pad;

dispensing a viscous conductive material on said flip-chip to define at least one conductive bump of a selected configuration exhibiting a height-to-width ratio of at least approximately 3 to 1, said at least one conductive bump in electrical communication with said at least one bond pad of said flip-chip and including a first surface adjacent said flip-chip and a second surface opposite said first surface; and

inverting said flip-chip without substantial lateral confinement of said viscous conductive material and maintaining said flip-chip in an inverted position at least until said conductive material substantially stabilizes so as to exhibit a desired stable shape and lateral boundary substantially defining sizes of said first and second surfaces of said at least one conductive bump and wherein a substantial portion of said second surface of said at least one conductive bump exhibits a generally planar configuration.

16. (Previously Amended) The flip-chip of claim 15, wherein dispensing said viscous conductive material includes:

placing a template, including at least one aperture, on said flip-chip;

depositing a conductive material into said template aperture; and

removing said template prior to inverting said flip-chip.

25. The semiconductor substrate of claim 7, wherein said viscous adhesive material of said at least one adhesive patch comprises at least one of the group consisting of a polyimide, a phenolic resin, a thermoplastic, and a thermosetting plastic.

26. The semiconductor substrate of claim 7, wherein said at least one adhesive patch comprises at least one lateral edge exhibiting an angle of repose of at least approximately 20 degrees.

27. The semiconductor substrate of claim 7, wherein said at least one adhesive patch comprises at least one trailing edge exhibiting an angle of repose of at least approximately 13 degrees.

28. The semiconductor substrate of claim 7, wherein said at least one adhesive patch comprises at least one leading edge exhibiting an angle of repose of at least approximately 20 degrees.

29. The semiconductor substrate of claim 7, wherein said at least one adhesive patch comprises a height-to-width ratio of at least approximately 3 to 1.

30. The semiconductor substrate of claim 8, wherein said template including at least one aperture comprises a print screen including a plurality of apertures.

31. The semiconductor substrate of claim 8, wherein said template including at least one aperture comprises a stencil including a plurality of apertures.

38. The flip-chip of claim 15, wherein said at least one conductive bump comprises at least one lateral edge exhibiting an angle of repose of at least approximately 20 degrees.

39. The flip-chip of claim 15, wherein said at least one conductive bump comprises at least one trailing edge exhibiting an angle of repose of at least approximately 12 degrees.

40. The flip-chip of claim 15, wherein said at least one conductive bump comprises at least one leading edge exhibiting an angle of repose of at least approximately 20 degrees.

41. The flip-chip of claim 15, wherein said conductive material of said at least one conductive bump comprises a conductive polymer material.

42. The flip-chip of claim 15, wherein said viscous conductive material of said at least one conductive bump comprises at least one of the group consisting of a polyimide, a phenolic resin, a thermoplastic, and a thermosetting plastic.

43. The flip-chip of claim 16, wherein said template having at least one aperture comprises a print screen including a plurality of apertures.

44. The flip-chip of claim 16, wherein said template having at least one aperture comprises a stencil including a plurality of apertures.

46. A semiconductor substrate including at least one adhesive patch comprised of a viscous adhesive material, the at least one adhesive patch including a first surface adjacent said semiconductor substrate and a second surface opposite said first surface, said second surface exhibiting a generally planar portion over a substantial portion thereof.

47. (Previously Amended) The semiconductor substrate of claim 46, wherein said viscous adhesive material comprises at least one of the group consisting of a polyimide, a phenolic resin, a thermoplastic, and a thermosetting plastic.

48. (Previously Amended) The semiconductor substrate of claim 46, wherein said at least one adhesive patch comprises at least one lateral edge exhibiting an angle of repose of at least approximately 20 degrees.

49. (Previously Amended) The semiconductor substrate of claim 46, wherein said at least one adhesive patch comprises at least one trailing edge exhibiting an angle of repose of at least approximately 13 degrees.

50. (Previously Amended) The semiconductor substrate of claim 46, wherein said at least one adhesive patch comprises at least one leading edge exhibiting an angle of repose of at least approximately 20 degrees.

51. (Previously Amended) The semiconductor substrate of claim 46, wherein said at least one adhesive patch exhibits a height-to-width ratio of at least approximately 3 to 1.

57. A flip-chip including at least one conductive bump comprised of a viscous conductive material, the at least one conductive bump exhibiting a height-to-width ratio of at least approximately 3 to 1 and including a first surface adjacent said flip-chip and a second surface opposite said first surface, said second surface exhibiting a generally planar portion over a substantial portion thereof.

58. (Previously Amended) The flip-chip of claim 57, wherein said viscous conductive material of said at least one conductive bump comprises at least one of the group consisting of a polyimide, a phenolic resin, a thermoplastic, and a thermosetting plastic.

59. (Previously Amended) The flip-chip of claim 57, wherein said at least one conductive bump comprises at least one lateral edge exhibiting an angle of repose of at least approximately 20 degrees.

60. (Previously Amended) The flip-chip of claim 57, wherein said at least one conductive bump comprises at least one trailing edge exhibiting an angle of repose of at least approximately 13 degrees.

61. (Previously Amended) The flip-chip of claim 57, wherein said at least one conductive bump comprises at least one leading edge exhibiting an angle of repose of at least approximately 20 degrees.

REMARKS

No new matter has been added. The Applicants request entry of the foregoing amendment prior to examination of the application on the merits.

Respectfully submitted,

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Date: September 5, 2001

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